H.264 EBH

Highest quality video encoding implemented

H.264EBH is a highly integrated IP core specifically designed for highest quality video compression. With H.264 EBH, encoding high definition content requires 0 processor resources. Further, advanced system prototyping support and flexible SoC integration are key features in our design mentality.

Maximizing your performance H.264 EBH is in full compliance to ISO/IEC 14496-10 (ITU-T H.264 or MPEG-4 part10/AVC) video coding standard. It is designed to offer the maximum level of performance and compression quality at the lowest possible bit-rate, with minimal power and silicon requirements. Supported resolutions range from QCIF(176x120) up to 2048x2048, at 30 fps or more. Multi-core instantiation is also possible in order to offer multichannel encoding and maximum performance up to real time full HD.

Minimal host intervention Our core accepts standard digital video input and requires minimal host intervention, constrained to typical register access, in order to produce fully formed NAL video streams. It can be interfaced to any host through a generic system interface. Furthermore, it is efficiently utilized both in high volume SoCs and niche market FPGA based developments covering a large variety of multimedia products and platforms.

ASIC or FPGA - It's your choice. Whether your interest is in ASIC or FPGA based solutions, H.264 EBH can be configured to meet both technology requirements. Our core's architecture allows flexible and highly competitive combination of encoding features in order to offer maximum video quality solutions tailored for different FPGA devices or SoC platforms. H.264 EBH supports HDTV video compression (720p) even when implemented in the modest VLSI (0.18um) technology. For FPGA implementations, full D1 resolution at 30 frames per second with a single core is supported.

Made for you. H.264 EBH is for you if you are looking for advanced encoding solutions for:

- Mobile Video Applications
- Video Surveillance/ IP cameras
- Digital Video Recorders
- Set-Top-Boxes
- Video Conferencing
- HDTV

About GDT

GDT is a system design house focused on designing Silicon Intellectual Property cores for multimedia communications systems. Our portfolio encompasses complete high technology cores for video compression, encoding and networking. Our role can be an IP vendor, design contractor, ASIC/FPGA/system integrator – always adapting to your needs.

We at GDT are proud to be delivering high-value, advanced ICT technology

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H.264 EBH Features

- ISO/IEC 14496-10 (MPEG-4 Part 10), AVC/H.264 Compliant video encoder
- Baseline Profile support
- Single core max frame resolution up to 2048x2048
- Single Core throughput
  - 352x288 x 30 fps @ 20 MHz
  - 720x576/480 x 25/30 fps @ 65 MHz
  - 1280x720 x 20 fps @ 125 MHz
- I and P frame types supported
- CAVLC Entropy coding
- Variable bit-rate, up to 80 Mbps
- Programmable GOP
- Control “quality factor”/ quantization configuration down to Macroblock level
- Selection Mode Decision “Low Complexity Lagrange”
- Configurable external interfaces are video source input, video RAM and microprocessor interface. For example, supported are:
  - Digital Image Sensor interface (CCIR-656 compliant)
  - DRAM memory interface
  - AMBA 2.0 AHB Slave interface

Motion Estimation features

- Half and Quarter Pel support
- Search region : +/- 16x16 Pel (can be extended)
- Macroblock partition possible, up to 4 Motion Vectors per MB (can be extended to 16 for low resolution)
- De-blocking Filter operation supported
- Rate statistics report per data packet
- Fully static synchronous design
- Single Clock Domain

Intra prediction features

- 16x16 All modes
- 4x4 All modes

H.264 EBH Deliverables

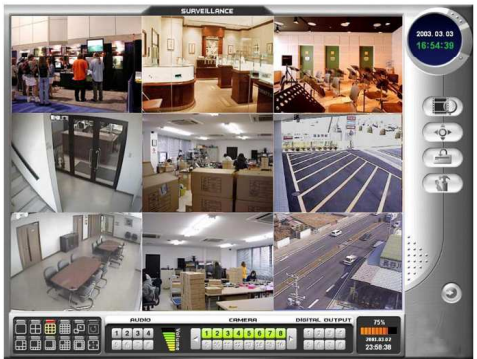
Encoder Core

- VHDL RTL source code
- Synthesized netlist
- FPGA PROM file
- Synthesis scripts
- Complete VHDL testbench
- Bit accurate model
- Encoder documentation and system integration guide

Standard and embedded Linux driver supporting 2.4 and 2.6 Kernels

PLUS for integration and verification: Hardware demo board

- AVNET Virtex-4 LX FPGA Virtex-4
- USB system interface
- H.264 encoder configuration s/w



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